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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/617,114	07/09/2003	Jian-gang Weng	200208154-1	2605

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EXAMINER	
KEBEDE, BROOK	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 06/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/617,114	WENG ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears n the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,8-24 and 27-32* is/are rejected.

7)☒ Claim(s) *5-7,25 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/9/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

1. Claims 1-32 are pending in the application.

2. Claims 1-32 are treated on the merits as set forth herein below.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-4, 8-10, 12-17, 29, and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Hirai et al. (US/2003/0047729).

FIG. 1 (b)

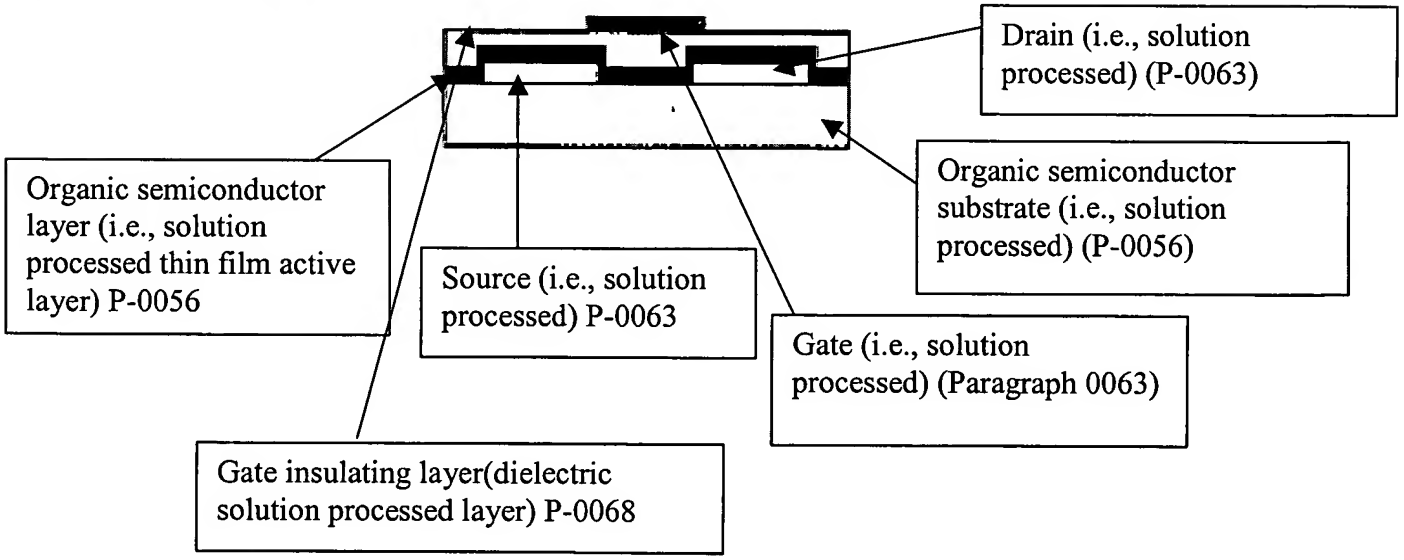


FIG. 1 (e)

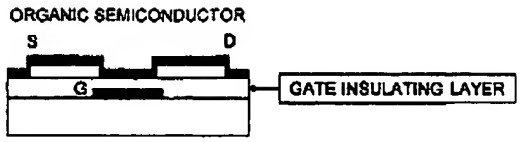
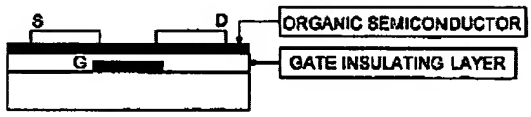


FIG. 1 (f)



Re claim 1, as shown in Figs. 1(b), 1(e), and 1(f) above, Hirai et al. disclose a solution-processed thin film transistor formation method, comprising steps of: forming conductive solution-processed thin film contacts (i.e., the source **S** and drain **D** contacts as shown in Figs. 1(b) , 1(e) and (f)) (also see Figs. 1(a) –f 1(f), semiconductor solution-processed thin film active regions (i.e., channel regions) (see Page 1 Paragraph 0012), and dielectric solution-processed thin film isolations (i.e., gate insulating layer) in a sequence and organization to form a solution-processed thin film structure capable of transistor operation (i.e., gate electrode G and source S and drain D), and selectively ablating one or more of the conductive solution-processed thin film contacts (see Page 5, Paragraph 0064), the semiconductor solution-processed thin film active regions and the dielectric solution-processed thin film isolations to pattern or complete patterning of a material being selectively ablated, wherein the step of selectively ablating is carried out during or after the step of forming (see Figs. 1(a) – 1(f); (see Page 3, Paragraph 0056 through Page 9, Paragraph 0134).

Re claim 2, as applied to claim 1 above, Hirai et al. disclose all the claimed limitations including the limitation wherein the step of selectively ablating is applied to complete patterning of a material roughly patterned when deposited (see Page 5, Paragraph 0064).

Re claim 3, as applied to claim 2 above, Hirai et al. disclose all the claimed limitations including the limitation wherein the material roughly patterned when deposited is patterned as a result of an inkjet deposition process (see Page 5, Paragraph 0064).

Re claim 4, as applied to claim 2 above, Hirai et al. disclose all the claimed limitations including the limitation wherein the material roughly patterned when deposited is patterned as a result of a spin coat deposition process (see Page 4, Paragraph 0061)

Re claim 8, as applied to claim 1 above, Hirai et al. disclose all the claimed limitations including the limitation wherein the steps of forming and ablating comprises, depositing drain (D) and source (S) conductive solution-processed thin film material (Fig. 1(b)) upon a substrate (Fig. 1(b)), selectively ablating a transistor channel in the drain and source conductive solution-processed thin films to form drain and source contacts (see Fig. 1(b)); depositing active region semiconductor solution-processed thin film material (see Fig. 1(b) above) over the drain and source contacts and the substrate (Fig.(1b)); depositing isolation region dielectric solution-processed thin film material over the semiconductor solution-processed thin film material; and depositing gate conductive solution- processed thin film material upon the isolation region dielectric to form a gate contact (see Fig. (1b); and Page 3, Paragraph 0056 through Page 9, Paragraph 0134).

Re claim 9, as applied to claim 8 above, Hirai et al. disclose all the claimed limitations including the limitation wherein the steps of depositing drain and source conductive solution-processed thin film material and depositing gate conductive solution-processed thin film material comprise inkjet printing conductive solution-processed thin film material (see Page 5, Paragraph 0064).

Re claim 10, as applied to claim 9 above, Hirai et al. disclose all the claimed limitations including the limitation wherein said step of depositing active region semiconductor solution-processed thin film material comprises spin coating semiconductor solution-processed thin film material; and the step of depositing isolation region dielectric solution-processed thin film material comprises spin coating dielectric solution-processed thin film material (see Page 3, Paragraph 0056 through Page 9, Paragraph 0134).

Re claim 12, as applied to claim 1 above, Hirai et al. disclose all the claimed limitations including the limitation wherein the steps of forming and ablating comprises, depositing gate conductive solution-processed thin film material upon a substrate (see Fig. 1(f) above); depositing isolation region dielectric solution-processed thin film material over the gate conductive solution-processed thin film material and the substrate (see Fig. 1(f)); depositing active region semiconductor solution-processed thin film material over the isolation region dielectric (see Fig. 1(f)); depositing drain (D) and source (S) conductive solution-processed thin film material upon the active region semiconductor solution-processed thin film material, and selectively ablating a transistor channel in the drain and source conductive solution-processed thin film material to form drain and source contacts (see Fig. 1(f); and Page 3, Paragraph 0056 through Page 9, Paragraph 0134).

Re claim 13, as applied to claim 12 above, Hirai et al. disclose all the claimed limitations including the limitation wherein said steps of depositing drain and source conductive solution-processed thin films and depositing gate conductive solution-processed thin film materials comprise inkjet printing conductive solution-processed thin film material (see Page 5, Paragraph 0064)

Re claim 14, as applied to claim 13 above, Hirai et al. disclose all the claimed limitations including the limitation wherein the step of depositing active region semiconductor solution-processed thin film material comprises spin coating semiconductor solution-processed thin film material, and the step of depositing isolation region dielectric solution-processed thin film material comprises spin coating dielectric solution-processed thin film material (see Page 4, Paragraph 0061).

Re claim 15, as applied to claim 1 above, Hirai et al. disclose all the claimed limitations including the limitation wherein the steps of forming and ablating comprises, depositing gate conductive solution-processed thin film material upon a substrate (see Fig. 1(e)); depositing isolation region dielectric solution-processed thin film material over the gate conductive solution-processed thin film material and the substrate (see Fig. 1(e)); depositing drain and source conductive solution-processed thin film material upon the isolation region dielectric solution-processed thin film material (see Fig. 1(e)); selectively ablating a transistor channel in the drain and source conductive solution-processed thin film material to form drain and source contacts, and depositing active region semiconductor solution-processed thin film material over the drain and source conductive solution-processed thin film material and the isolation dielectric (see Fig. 1(e) and Page 3, Paragraph 0056 through Page 9, Paragraph 0134).

Re claim 16, as applied to claim 15 above, Hirai et al. disclose all the claimed limitations including the limitation wherein the steps of depositing source and source conductive solution-processed thin films and depositing gate conductive solution-processed thin film material comprise inkjet printing conductive solution-processed thin film material (see Page 5, Paragraph 0064).

Re claim 17, as applied to claim 16 above, Hirai et al. disclose all the claimed limitations including the limitation wherein the step of depositing active region semiconductor solution-processed thin film material comprises spin coating semiconductor solution-processed thin film material; and said step of depositing isolation region dielectric solution-processed thin film material comprises spin coating dielectric solution-processed thin film material (see Page 4, Paragraph 0061).

Re claim 29, Hirai et al. disclose a solution-processed thin film transistor including drain, source and gate contacts formed of conductive solution-processed thin film materials (see Fig. 1(b), a semiconductor solution-processed thin film material active region contacting the drain and source contacts (see Fig. 1(b)) and isolated from the gate contact by a dielectric solution-processed thin film material (see Fig. 1(b)), the transistor being formed by a process comprising, depositing in a rough pattern, the drain and source contacts, and refining the rough pattern by selective laser ablation of the drain and source contacts (see Fig. (1b); and Page 3, Paragraph 0056 through Page 9, Paragraph 0134).

Re claim 30, as applied to claim 29 above, Hirai et al. disclose all the claimed limitations including the limitation wherein the step of refining creates a transistor channel (see Fig. 1(b) and Page 5, Paragraph 0064).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai et al. (US/2003/0047729).

Re claim 11, as applied to claim 8 in Paragraph 8 above, Hirai et al. disclose forming a channel length having 20 μm wide (i.e., outside the claimed channel length range of 5 μm or less) (see Fig. (1b); and Page 11, Paragraph 0175).

However, such channel length would have been formed by one of ordinary skill in the art by routine optimization in order to achieve the desired device size and performance.

One of ordinary skill in the art would have motivated to form the claimed channel length by routine optimization in order to achieve the desired device size and performance.

Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are

otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed channel length or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

7. Claims 18-24, 27, 28, 31, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai et al. (US/2003/0047729), as applied in Paragraph 5 above, in view of Kian et al. (US/6,602,790).

Re claim 18, as applied to claim 1 in Paragraph 4 above, Hirai et al. disclose all the claimed limitations including the limitation wherein the step leaser ablating of the solution processed layers (see Fig. 1(b), 1(e), and 1(f); and Page 5, Paragraph 0064).

Although it is within the scope Hirai et al. disclosure, Hirai et al. do not specifically disclose selective ablating uses a laser wavelength tuned to be absorbed by material being ablated and to minimally damage material underlying material being ablated.

Kian et al. disclose selectively ablating multilayered conductor/substrate structure using a laser wavelength tuned to be absorbed by material being ablated and to minimally damage material underlying material being ablated (see Col. 11, line 15 through Col. 12, line 65; Col. 19, line 8-67 through Col 20, line 13; Fig. 14). Kian et al. further disclose that "the typical plastic substrate, as compared to glass, has a surface topology with point-to-point variations both on a

local scale and over a larger area. Surface variations on the order of several micro-meters are common. Layers formed over the plastic substrate may have a wavy surface or other surface variation. Generally the UV irradiation process is controlled to avoid ablating the plastic substrate and to leave a protective layer which is sufficiently thick to perform its protective function. Thus, in a preferred embodiment, the depth of focus of the laser is selected/controlled to be sufficiently large to take into account the above-described surface variabilities." (see Col. 19, line 66 through Col. 20, line 13).

One of ordinary skill in the art would have been motivated to use the laser selective ablating uses a laser wavelength tuned to be absorbed by material being ablated and to minimally damage material underlying material being ablated because the radiation can be controlled and ablating (etching) of the substrate or underlying layer can be avoided.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Hirai et al. reference with selective ablating uses a laser wavelength tuned to be absorbed by material being ablated and to minimally damage material underlying material being ablated as taught by Kian et al. because the radiation can be controlled and ablating (etching) of the substrate or underlying layer can be avoided.

Re claim 19, as applied to claim 1 in Paragraph 4 above, Hirai et al. disclose all the claimed limitations including the limitation selectively ablating of the solution processed conducive material to form source, drain, and gate contacts (see Fig. 1(b), 1(e), and 1(f); and Page 5, Paragraph 0064).

Although it is within the scope of Hirai et al. disclosure, Hirai et al. do not specifically disclose wherein the step of selectively ablating is conducted through an optical mask to ablate multiple features simultaneously.

Kian et al. disclose conducting of selective ablating through an optical mask (1408) (see Fig. 14) in order to form multiple features simultaneously (see Col. 11, line 15 through Col. 12, line 65; Col. 19, line 8-67 through Col 20, line 13; Fig. 14).

One of ordinary skill would have been motivated to perform selective ablating trough an optical mask in order to form a desired pattern future on the film.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Hirai et al. reference with selectively ablating is conducted through an optical mask as taught by Kian et al. in order to form a desired pattern futures on the film.

Re claim 20, as applied to claim 1 in Paragraph 4 above, Hirai et al. disclose all the claimed limitations including the limitation selectively ablating of the solution processed conducive material to form source, drain, and gate contacts (see Fig. 1(b), 1(e), and 1(f); and Page 5, Paragraph 0064).

However, Hirai et al. do not specifically disclose the selectively ablating is carried out while varying one or both of a laser wavelength and intensity.

Kian et al. disclose selectively ablating of the conducive layer such as ITO layer and varying the wavelength the laser light in order to determine the optimum wavelength for particular ablating process (see Col. 11, line 64 – Col. 18 line 5).

One of ordinary skill would have been motivated to perform selective ablating while varying of a laser wavelength in order in order to determine the optimum wavelength for particular ablating process.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Hirai et al. reference with selectively

ablating while varying of a laser wavelength as taught by Kian et al. in order in order to determine the optimum wavelength for particular ablating process.

Re claim 21, Hirai et al. disclose a solution-processed thin film transistor formation method, comprising steps of: forming solution-processed thin film layers into a transistor structure (see Figs. 1(a) – 1(f)); during the forming, patterning portions of the transistor structure via laser ablation (see Figs. 1(a)-1(f); and Page 5, Paragraph 0064).

Although it is within the scope Hirai et al. disclosure, Hirai et al. do not specifically disclose selective ablating uses a laser wavelength tuned to be absorbed by material being ablated and to minimally damage material underlying material being ablated.

Kian et al. disclose selectively ablating multilayered conductor/substrate structure using a laser wavelength tuned to be absorbed by material being ablated and to minimally damage material underlying material being ablated (see Col. 11, line 15 through Col. 12, line 65; Col. 19, line 8-67 through Col 20, line 13; Fig. 14). Kian et al. further disclose that "the typical plastic substrate, as compared to glass, has a surface topology with point-to-point variations both on a local scale and over a larger area. Surface variations on the order of several micro-meters are common. Layers formed over the plastic substrate may have a wavy surface or other surface variation. Generally the UV irradiation process is controlled to avoid ablating the plastic substrate and to leave a protective layer which is sufficiently thick to perform its protective function. Thus, in a preferred embodiment, the depth of focus of the laser is selected/controlled to be sufficiently large to take into account the above-described surface variabilities." (see Col. 19, line 66 through Col. 20, line 13).

One of ordinary skill in the art would have been motivated to use the laser selective ablating uses a laser wavelength tuned to be absorbed by material being ablated and to minimally

damage material underlying material being ablated because the radiation can be controlled and ablating (etching) of the substrate or underlying layer can be avoided.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Hirai et al. reference with selective ablating uses a laser wavelength tuned to be absorbed by material being ablated and to minimally damage material underlying material being ablated as taught by Kian et al. because the radiation can be controlled and ablating (etching) of the substrate or underlying layer can be avoided.

Re claim 22, as applied to claim 21 above, both Hirai et al. and Kian et al. in combination disclose all the claimed limitations including the limitation wherein said step of patterning is applied to complete patterning of a material roughly patterned when deposited (see Hirai et al. Figs. 1(a) – 1(f) and Kian et al. Col. 19, line 66 through Col. 20, line 13).

Re claim 23, as applied to claim 22 above, both Hirai et al. and Kian et al. in combination disclose all the claimed limitations including the limitation wherein the material roughly patterned when deposited is patterned as a result of an inkjet deposition process (Hirai et al. Figs. 1(a) – 1(f), Page 5, Paragraph 0064; and Kian et al. Col. 19, line 66 through Col. 20, line 13).

Re claim 24, as applied to claim 22 above, both Hirai et al. and Kian et al. in combination disclose all the claimed limitations including the limitation wherein the material roughly patterned when deposited is patterned as a result of a spin coat deposition process (Hirai et al. Figs. 1(a) – 1(f), Page 4, Paragraph 0061; and Kian et al. Col. 19, line 66 through Col. 20, line 13).

Re claim 27, as applied to claim 21 above, both Hirai et al. and Kian et al. in combination disclose all the claimed limitations including the limitation wherein said step of patterning is conducted through an optical mask to ablate multiple features simultaneously (see Hirai et al.

Figs. 1(a)-1(f); see Kian et al Col. 11, line 15 through Col. 12, line 65; Col. 19, line 8-67 through Col 20, line 13; Fig. 14).

Re claim 28, as applied to claim 21 above, both Hirai et al. and Kian et al. in combination disclose all the claimed limitations including the limitation wherein said step of patterning is carried out while varying one or both of a laser wavelength and intensity simultaneously (see Hirai et al. Figs. 1(a)-1(f); see Kian et al. see Col. 11, line 64 – Col. 18 line 5).

Re claim 31, as applied to claim 29 in Paragraph 4 above, Hirai et al. disclose all the claimed limitations including the limitation selectively ablating of the solution processed conducive material to form source, drain, and gate contacts (see Fig. 1(b), 1(e), and 1(f); and Page 5, Paragraph 0064).

Although it is within the scope of Hirai et al. disclosure, Hirai et al. do not specifically disclose wherein the step of selectively ablating is conducted through an optical mask to ablate multiple features simultaneously.

Kian et al. disclose conducting of selective ablating through an optical mask (1408) (see Fig. 14) in order to form multiple features simultaneously (see Col. 11, line 15 through Col. 12, line 65; Col. 19, line 8-67 through Col 20, line 13; Fig. 14).

One of ordinary skill would have been motivated to perform selective ablating trough an optical mask in order to form a desired pattern future on the film.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Hirai et al. reference with selectively ablating is conducted through an optical mask as taught by Kian et al. in order to form a desired pattern futures on the film.

Re claim 32, as applied to claim 29 in Paragraph 4 above, Hirai et al. disclose all the claimed limitations including the limitation selectively ablating of the solution processed conducive material to form source, drain, and gate contacts (see Fig. 1(b), 1(e), and 1(f); and Page 5, Paragraph 0064).

However, Hirai et al. do not specifically disclose the selectively ablating is carried out while varying one or both of a laser wavelength and intensity.

Kian et al. disclose selectively ablating of the conducive layer such as ITO layer and varying the wavelength the laser light in order to determine the optimum wavelength for particular ablating process (see Col. 11, line 64 – Col. 18 line 5).

One of ordinary skill would have been motivated to perform selective ablating while varying of a laser wavelength in order in order to determine the optimum wavelength for particular ablating process.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Hirai et al. reference with selectively ablating while varying of a laser wavelength as taught by Kian et al. in order in order to determine the optimum wavelength for particular ablating process.

Allowable Subject Matter

8. Claims 5-7, 25, and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record neither anticipates nor renders obvious the claimed subject matter of the instant application as a whole either taken alone or in combination, in particular, prior art

of record does not teach "forming device isolations by ablating material between structures," as recited in claim 5, and "forming device isolations by ablating material between structures," as recited in claim 25.

Claims 6 and 7 also would be allowable being dependent upon claim 5; and Claim 26 also would be allowable being dependent upon claim 25 respectively.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure Bradley, Jr. et al. (US/5,824,374), Dimitrakopoulos et al. (US/5,981,970), Gleskova et al. (US/6,080,606), Sturm et al. (US/6,087,196), Sirringaus et al. (US/2003/0059984), Tessler et al. (US/6,603,139), Hirai (US/2003/0160235), Hirai et al. (US/2003/0211649), Aramaki et al. (US/2003/0226996), and Mognsen (US/6,697,694) also disclose method of fabricating solution processed thin film transistors.

Remarks

11. Paper copies of the recited U.S. Patents and Patent Application Publications that listed in PTO-892 are not mailed to applicant(s) due to implementation of Electronic Maintenance of Official Patent Application(s) Records. However, the references can be downloaded through the PAIR system.

Correspondence

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brook Kebede
Examiner
Art Unit 2823

Brook Kebede

BK
June 8, 2004